REMARKS

This amendment is in response to the Office Action dated July 21, 2009 (the "Office Action"). Claims 3, 8-10, 16, 20, 21, 24-46, and 51-55 have been canceled without prejudice or disclaimer. Claims 1, 4, 5, 7, 14, 17, 18, 22, 23, 50, and 56 have been amended. Claim 57-61 have been added. No new matter has been added. Support for the new claims and the claim amendments may be found at least at paragraphs [0018], [0032], and [0039]-[0040].

Claim Rejections – 35 U.S.C. § 112

Claims 1-55 are rejected under 35 U.S.C. § 112, second paragraph. Specifically, the Office Action states, "The independent claims recite a first memory and a second memory. It is not clear what defines a memory or how to distinguish one memory from another. For the purpose of examination the examiner assumes each address location in a memory may be read as a separate memory." Office Action, p. 2. Applicants respectfully disagree. As an initial matter, the Office Action does not accurately quote the claim language. For example, prior to the amendments presented herein, claim 1 recited, "a first memory device" and "a second memory device" (emphasis added). Thus, claim 1 clearly includes two separated memory devices, not merely two separate memory locations.

Further, as amended, the claims further clarify issues related to the memory devices. For example, claim 1 recites "a first memory device external to a processor" and "a second memory device internal to the processor." In another example, claim 14 recites that "the first memory device is coupled to the processor via a bus" and that "the second memory device is internal to the processor." In yet another example, claim 56 recites "a first memory device coupled to a processor by a bus" and "a second memory device integral with the processor." Accordingly, the language of independent claims 1, 14 and 56 clearly point out and distinctly claim separate memory devices and comply with the requirements of 35 U.S.C. §112, second paragraph.

The Office Action further states, "As per claims 48 and 49, the claims recite that the first memory includes a flash device, and the second memory includes a RAM device. It is again not clear what separates one memory from another as applicant is already stating in the claims that a 'first memory device' may comprise more than just a single flash memory device or RAM memory device. It is not clear what defines a 'memory'." Office Action, pp. 2-3. Applicants

respectfully disagree. The Office Action has again misquoted the claims. In particular, claim 48 recites that "the first memory device is a FLASH memory device" (emphasis added). Further, claim 49 recite that "the second memory device is a RAM memory device" (emphasis added). Thus, the claims 48 and 49 (in combination with claim 1 from which claims 48 and 49 depend) clearly include a first memory device that is a FLASH memory device and a second memory device that is a RAM memory device. Accordingly, claims 48 and 49 comply with the requirements of 35 U.S.C. §112, second paragraph.

The Office Action also rejects claim 51 under 35 U.S.C. §112, second paragraph. Office Action, p. 3. Claim 51 has been canceled without prejudice or disclaimer rendering the rejection of claim 51 moot.

The Office Action states, "As per claims 14-23, 46, 53-55, it is not clear how the disclosed invention defines a called party responding or not responding to a message. How does the system differentiate between an actual person responding and the voice of a voicemail answering system?" Office Action, p. 3. Claims 16, 20, 21, 46, and 53-55 have been canceled without prejudice of disclaimer, rendering the rejections of claims 16, 20, 21, 46, and 53-55 moot. Claim 14, from which claims 15, 17-19, 22, and 23 depend, has been amended. Accordingly, claims 14, 15, 17-19, 22, and 23 comply with the requirements of 35 U.S.C. §112, second paragraph.

Claim Rejections – 35 U.S.C. § 103

Claims 1, 2, 4-7, 11-15, 17-19, and 21-23 are Allowable

The Office has rejected claims 1, 2, 4-7, 11-13, 15, 17-19, 21-23, 44, 46-50, and 53-56, under 35 U.S.C. § 103(a), as being unpatentable over U.S. Patent Application Publication No. 2004/0017794 ("Trachewsky") in view of U.S. Patent Application Publication No. 2002/0161907 ("Moon"). Applicants respectfully traverse the rejections.

Applicants respectfully note the Office Action has not presented a rejection of claim 14 under 35 U.S.C. §103. Thus, no prima facie case of obviousness has been established with respect to claim 14. Accordingly, since the rejections of claim 14 under 35 U.S.C. §112, second paragraph have been overcome, Applicants respectfully request allowance of claim 14. However, if the omission of claim 14 from the rejections under 35 U.S.C. §103 was

unintentional, Applicants respectfully request that, if the Office later presents a rejection of claim 14 such rejection be presented in a Non-Final Office Action since the Applicants have not been provided an opportunity to respond in this Non-Final Office Action.

Applicants further respectfully note that since no prima facie case of obviousness has been established with respect to claim 14, no prima facie case of obviousness has been established with respect to claims 15-19, 22, 23, and 57-60, which depend from claim 14. Thus, although the Office Action purports to reject claims 15-19, 22, 23, and 57-60 as unpatentable over Trachewsky in view of Moon, such rejections are improper since the combination of Trachewsky and Moon has not been shown to teach or suggest each and every element of claim 14. Accordingly, claims 14-19, 22, 23, and 57-60 are allowable. However, to expedite examination of the application, arguments are presented herein demonstrating that claims 14-19, 22, 23, and 57-60 are allowable over Trachewsky in view of Moon.

Claims 1, 2, 4-7, 11-13, and 47-49

The cited portions of Trachewsky and Moon fail to disclose or suggest the specific combination of claim 1. For example, the cited portions of Trachewsky and Moon fail to disclose or suggest a telephone gateway device that executes first virtual machine instructions (retrieved from a first memory device external to a processor) to instantiate a first finite state machine and to store a first state table based on template state data associated with the first virtual machine instructions at the second memory device (internal to the processor), where the first finite state machine and the first state table specify at least a portion of the first telecommunication protocol, as in claim 1.

The Office Action admits that Trachewsky fails to disclose implementation of a gateway using a virtual machine, as in claim 1. Office Action, p. 4. Additionally, in contrast to claim 1, Trachewsky teaches a communication gateway supporting wireless local area network communications in multiple communication protocols and in multiple frequency bands. Trachewsky, Title. Trachewsky teaches using multiple baseband processors, where each baseband processor is formed to operate according to a respective protocol. Trachewsky, paragraph [0047]. Trachewsky further teaches a plurality of baseband processing cards, each of which performs digital processing according to a respective wireless protocol. Thus, each baseband processor and each baseband processing card of Trachewsky is dedicated to a particular protocol. The Office Action asserts that many of the elements of claim 1 are

"inherently" performed by the system disclosed by Trachewsky. Applicants respectfully traverse these assertions.

The burden is on the Office to show that an element is inherent: "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." MPEP § 2112.IV (quoting *Ex Parte Levy*, 17 U.S.P.Q. 2d 1461, 1464 (Bd. Pat. App. & Inter. 1990; emphasis in the original). Further, "[t]he fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.'" MPEP § 2112.IV (citations omitted; emphasis in the original). Respectfully, the Office Action fails to present extrinsic evidence that would make clear that "the CPU steps of claim 1" are necessarily present in the system disclosed by Trachewsky. For example, the Office Action does not provide any evidence that a processor of Trachewsky necessarily retrieves first virtual machine instructions from a first memory device external to the processor to instantiate a first finite state machine and to store a first state table based on template state data associated with the first virtual machine instructions at the second memory device internal to the processor, where the first finite state machine and the first state table specify at least a portion of the first telecommunication protocol. The Office Action also fails to cite any extrinsic evidence to suggest that the other elements of claim 1 that are not explicitly disclosed by Trachewsky are necessarily present. Accordingly, the cited portions of Trachewsky fail to disclose or suggest a telephone gateway device that executes first virtual machine instructions (retrieved from a first memory device external to a processor) to instantiate a first finite state machine and to store a first state table based on template state data associated with the first virtual machine instructions at the second memory device (internal to the processor), where the first finite state machine and the first state table specify at least a portion of the first telecommunication protocol, as in claim 1.

In further contrast to claim 1, Moon relates to an adaptive multi-protocol communication system. Moon, Title. The system of Moon includes a plurality of computer interface cards, where each of the computer interface cards sends and receives bit streams of a specific application protocol. Moon, Abstract. Thus, each computer interface card of Moon is dedicated to a particular protocol. Accordingly, the cited portions of Moon fail to disclose or suggest a telephone gateway device that executes first virtual machine instructions (retrieved from a first memory device external to a processor) to instantiate a first finite state machine and to store a first state table based on template state data associated with the first virtual machine instructions at the second memory device (internal to the processor), where the first finite state machine and the first state table specify at least a portion of the first telecommunication protocol, as in claim 1.

Hence, claim 1 is allowable. Claims 2, 4-7, 11-13 and 47-49 depend from claim 1. Accordingly, claims 2, 4-7, 11-13 and 47-49 are allowable, at least by virtue of their dependence from claim 1.

Claims 14, 15, 17-19, 22, 23, and 57-60

The cited portions of Trachewsky and Moon fail to disclose or suggest the specific combination of claim 14. For example, the cited portions of Trachewsky and Moon fail to disclose or suggest initializing a first finite state machine using a first virtual machine instruction (read from a first memory device coupled to a processor), where the first telecommunication protocol template includes first template state data defining a first template state of the first finite state machine and storing the first template state at a second memory device of a telephony gateway device in a first state table, where the second memory device is internal to the processor, as in claim 14.

In the rejection of claim 1, the Office Action admits that Trachewsky fails to disclose implementation of a gateway using a virtual machine, as in claim 14. Office Action, p. 4. Additionally, in contrast to claim 14, Trachewsky teaches a communication gateway supporting wireless local area network communications in multiple communication protocols and in multiple frequency bands. Trachewsky, Title. Trachewsky teaches using multiple baseband processors, where each baseband processor is formed to operate according to a respective protocol. Trachewsky, paragraph [0047]. Trachewsky further teaches a plurality of baseband processing cards, each of which performs digital processing according to a respective wireless

protocol. Thus, each baseband processor and each baseband processing card of Trachewsky is dedicated to a particular protocol. In rejecting claim 1, the Office Action asserts that many of the elements of claim 1 are "inherently" performed by the system disclosed by Trachewsky. Applicants respectfully traverse these assertions since the Office has not met its burden of proof in providing extrinsic evidence making it clear that the elements of claim 1 (or of claim 14) are necessarily present in the system of Trachewsky. Accordingly, the cited portions of Trachewsky fail to disclose or suggest initializing a first finite state machine using a first virtual machine instruction (read from a first memory device coupled to a processor), where the first telecommunication protocol template includes first template state data defining a first template state of the first finite state machine and storing the first template state at a second memory device of a telephony gateway device in a first state table, where the second memory device is internal to the processor, as in claim 14.

In further contrast to claim 14, Moon relates to an adaptive multi-protocol communication system. Moon, Title. The system of Moon includes a plurality of computer interface cards, where each of the computer interface cards sends and receives bit streams of a specific application protocol. Moon, Abstract. Thus, each computer interface card of Moon is dedicated to a particular protocol. Accordingly, the cited portions of Moon fail to disclose or suggest initializing a first finite state machine using a first virtual machine instruction (read from a first memory device coupled to a processor), where the first telecommunication protocol template includes first template state data defining a first template state of the first finite state machine and storing the first template state at a second memory device of a telephony gateway device in a first state table, where the second memory device is internal to the processor, as in claim 14.

Hence, claim 14 is allowable. Claims 15, 17-19, 22, 23, and 57-60 depend from claim 14. Accordingly, claims 15, 17-19, 22, 23, and 57-60 are allowable, at least by virtue of their dependence from claim 14.

Further, the dependent claims include additional features that are not disclosed or suggested by the cited portions of Trachewsky and Moon. For example, the cited portions of Trachewsky and Moon fail to disclose or suggest that a second template state (of a second finite state machine) is determined based on a first finite state machine, as in claim 22. In another example, the cited portions of Trachewsky and Moon fail to disclose or suggest determining a

transition of a first finite state machine based on a second finite state machine, as in claim 23. In yet another example, the cited portions of Trachewsky and Moon fail to disclose or suggest sending a message to a called party in response to input, where updated template state is determined based on a response to the message, as in claim 57. In another example, the cited portions of Trachewsky and Moon fail to disclose or suggest that when no response to a message is received from a called party, an updated template state comprises a fast busy tone state, as in claim 58. In another example, the cited portions of Trachewsky and Moon fail to disclose or suggest that when a response to a message indicates that a telephony call has been answered, the method further comprises executing an init vocoder instruction, as in claim 59. In another example, the cited portions of Trachewsky and Moon fail to disclose or suggest that when a response to a message indicates that a telephony call has been answered, an updated template state comprises a voice state, as in claim 60. Accordingly, claims 22, 23, and 57-60 are allowable for at least these additional reasons.

Claim 56

The cited portions of Trachewsky and Moon fail to disclose or suggest the specific combination of claim 56. For example, the cited portions of Trachewsky and Moon fail to disclose or suggest a processor configured to execute first virtual machine instructions (read from a first memory device that is coupled to the processor by a bus) using first template state data to initialize the first finite state machine and to store an initial state table of the first finite state machine at a second memory device (integral with the processor), as in claim 56.

The Office Action admits that Trachewsky fails to disclose implementation of a gateway using a virtual machine, as in claim 56. Office Action, p. 4. Additionally, in contrast to claim 56, Trachewsky teaches a communication gateway supporting wireless local area network communications in multiple communication protocols and in multiple frequency bands. Trachewsky, Title. Trachewsky teaches using multiple baseband processors, where each baseband processor is formed to operate according to a respective protocol. Trachewsky, paragraph [0047]. Trachewsky further teaches a plurality of baseband processing cards, each of which performs digital processing according to a respective wireless protocol. Thus, each baseband processor and each baseband processing card of Trachewsky is dedicated to a particular protocol. The Office Action asserts that many of the elements of claim 56 are "inherently" performed by the system disclosed by Trachewsky. Applicants respectfully traverse

these assertions since the Office has not met its burden of proof in providing extrinsic evidence making it clear that the elements of claim 56 are necessarily present in the system of Trachewsky. Accordingly, the cited portions of Trachewsky fail to disclose or suggest a processor configured to execute first virtual machine instructions (read from a first memory device that is coupled to the processor by a bus) using first template state data to initialize the first finite state machine and to store an initial state table of the first finite state machine at a second memory device (integral with the processor), as in claim 56.

In further contrast to claim 56, Moon relates to an adaptive multi-protocol communication system. Moon, Title. The system of Moon includes a plurality of computer interface cards, where each of the computer interface cards sends and receives bit streams of a specific application protocol. Moon, Abstract. Thus, each computer interface card of Moon is dedicated to a particular protocol. Accordingly, the cited portions of Moon fail to disclose or suggest a processor configured to execute first virtual machine instructions (read from a first memory device that is coupled to the processor by a bus) using first template state data to initialize the first finite state machine and to store an initial state table of the first finite state machine at a second memory device (integral with the processor), as in claim 56.

Hence, claim 56 is allowable.

CONCLUSION

Applicants have pointed out specific features of the claims not disclosed, suggested, or rendered obvious by the cited portions of the references applied in the Office Action. Accordingly, Applicants respectfully request reconsideration and withdrawal of each of the rejections, as well as an indication of the allowability of each of the pending claims.

Any changes to the claims in this response, which have not been specifically noted to overcome a rejection based upon the cited art, should be considered to have been made for a purpose unrelated to patentability, and no estoppel should be deemed to attach thereto.

The Examiner is invited to contact the undersigned attorney at the telephone number listed below if such a call would in any way facilitate allowance of this application.

The Commissioner is hereby authorized to charge any fees, which may be required, or credit any overpayment, to Deposit Account Number 50-2469.

Respectfully submitted,

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Date

Jeffrey G. Toler, Reg. No. 38,342
Attorney for Applicant(s)
Toler Law Group, Intellectual Properties
8500 Bluffstone Cove, Suite A201
Austin, Texas 78759
(512) 327-5515 (phone)
(512) 327-5575 (fax)